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EXAMINER	
HSU, JONI	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,417	MAS ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *June 12, 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-29* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/18/03, 8/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on July 18, 2003 and August 27, 2003 were filed after the mailing date of the application on July 18, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. Applicant's arguments, see page 8, filed June 12, 2006, with respect to the objection to the specification have been fully considered and are persuasive. The objection to the specification has been withdrawn.

3. Applicant's arguments with respect to claims 1, 2, and 4-29 have been considered but are moot in view of the new ground(s) of rejection.

4. Applicant's arguments, see pages 9-10, filed June 12, 2006, with respect to the rejection(s) of claim(s) 1, 2, 4, and 5 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Wu (US006414689B1).

5. With regard to Claims 1, 2, 4, and 5, Applicant argues that Richards (US006756976B2), Glennon (US006359654B1), and Leung (US005900887A) do not teach activating pixels of a screen line associated with the address offset by a same pixel position offset value or activating pixels of a screen line associated with the row address based on the read states of the frame memory row associated with the address offset by a same pixel position offset value (page 9, paragraph 4).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Wu.

6. With regard to Claims 6-29, Applicant argues that Richards, Glennon, and Leung do not teach determining whether a second image to be displayed after the first image is substantially similar or identical to the first image and selectively activating the pixels to display the second image so that at least a portion of the second image is displayed offset in position on the screen from the position in which the first image was displayed (pages 10-11).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Choi (US 20030076332A1).

Claim Objections

7. Claim 8 is objected to because of the following informalities: Claim 8 recites "*an* position offset" where it should recite "*a* position offset". Appropriate correction is required.

8. Claim 26 objected to because of the following informalities: Claim 26 depends from Claim 24, and Claim 26 recites the phrase "the at least one third circuit." There is a lack of antecedent basis for the phrase "the at least one third circuit" in Claim 24 or any of the other intervening claims. Applicant is assumed to have meant that Claim 26 depends from Claim 25, since Claim 25 recites the phrase "at least one third circuit." Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 6-11, 13, 18-20, and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Choi (US 20030076332A1).

11. With regard to Claim 6, Choi discloses a method of displaying images using pixels, the method comprising selectively activating the pixels to display a first image on a screen (*sends the control signal, which causes the displayed image to move by one pixel*, [0036]); determining whether a second image to be displayed after the first image is substantially similar or identical

to the first image; and if the second image is substantially similar or identical to the first image, selectively activating the pixels to display the second image so that at least a portion of the second image is displayed offset in position on the screen from the position in which the first image was displayed (*The controller 104 judges whether the same image is displayed for a certain period of time, based on the comparison result. If the controller 104 judges that the same image is displayed for a certain period of time, it sends a control signal, according to which the position of the displayed image is moved*, [0035, 0036]).

12. With regard to Claim 7, Choi discloses that the offset in position is at least a width of one of the pixels (*move by one pixel*, [0036]).

13. With regard to Claim 8, Choi discloses that selectively activating the pixels to display the second image comprises displaying substantially the entire second image in a position offset from the position in which the first image was displayed (*position of the displayed image is moved*, [0035, 0036]).

14. With regard to Claim 9, Choi discloses that substantially the entire second image is displayed in a position offset by substantially a same distance (*position of the displayed image is moved*, [0035], *the displayed image is moved by one pixel*, 0036]).

15. With regard to Claim 10, Choi discloses determining whether a third image to be displayed after the second image is substantially similar or identical to the second image; and if

the third image is substantially similar or identical to the second image, selectively activating the pixels to display the third image so that at least a portion of the third image is displayed offset in position on the screen from the position in which the second image was displayed (*after the image is moved in the left direction by one pixel, if the controller 104 judges that the same image continues to be displayed for a certain period of time, the controller 104 sends the control signal, which causes the displayed image to move by one pixel*, [0037].

16. With regard to Claim 11, Choi discloses displaying a substantially similar or identical image at different pixel positions on the display at different times (*the displayed image is moved by one pixel in the left direction*, [0036], *after the image is moved in the left direction by one pixel, if the same image continues to be displayed for a certain period of time, the displayed image is moved by one pixel in the upper direction*, [0037-0040]).

17. With regard to Claim 13, Choi discloses that the substantially similar or identical image is displayed at different pixel positions on the display by being moved left, up, right, and down at different times such that the position of the image is changed in a cyclical manner ([0036-0039], *repeats the above operation*, [0040]).

18. With regard to Claim 18, Choi discloses a device for displaying an image, comprising at least one first circuit (101, 105 Figure 1) that activates pixels to display the image (*signal processor 101 converts the read signal into the display format and outputs it*, [0029], *displayed image is moved by one pixel*, [0036], *operation unit 105 operates the display unit 106 so that the*

image signal transmitted from the signal processor 101 can be displayed on a desired position of the display unit 106, [0041]); and at least one second circuit (104, 103) that determines whether the image is a substantially similar or identical image to a previously displayed image and, if so, provides position offset information to the at least one first circuit such that the image is displayed in an offset position with respect to the position at which the previously displayed image was displayed [0035, 0036].

19. With regard to Claim 19, Choi discloses a memory (102, Figure 1) that stores the image (*image signal stored in the memory 102*, [0029]).

20. With regard to Claim 20, Choi discloses that the at least one second circuit (104, 103, Figure 1) comprises a processor (103); and a dedicated control circuit (104) that receives a control signal from the processor and determines, based on the control signal, position offset information (*The controller 104 judges whether the same image is displayed for a certain period of time, based on the comparison result transmitted by the comparator 103. If the controller 104 judges that the same image is displayed for a certain period of time, it sends a control signal, according to which the position of the displayed image is moved based on the condition information about the movement range*, [0036]).

21. With regard to Claim 22, Choi discloses that the at least one second circuit (104, 103, Figure 1) determines whether the image is substantially similar or identical image to images that have previously been displayed for many successive frames and, if so, provides the position

offset information to the at least one first circuit (105) such that the image is displayed in an offset position with respect to the position in which at least one of the images was displayed (*the controller sends a control signal, according to which the position of the displayed image is moved, to the operation unit 105*, [0035-0040]).

22. Thus, it reasonably appears that Choi describes or discloses every element of Claims 6-11, 13, 18-20, and 22 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

25. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Richards (US006756976B2) in view of Glennon (US006359654B1), further in view of Wu (US006414689B1).

Richards describes a method for displaying an image by activation of pixels of an array screen based on an image stored in digital form in memory point rows of a frame memory, comprising a normal display mode comprising, for the display of a frame, the steps of: (a) providing a succession of row addresses associated with rows of the frame memory (310, Figure 2a) (Col. 5, line 65-Col. 6, line 4; Col. 13, lines 45-51); (b) successively reading the states of memory points of the rows associated with the row addresses (Col. 5, line 65-Col. 6, line 4; Col. 2, lines 43-48); and (c) activating, for each row address, pixels of a line associated with the row address based on the read states of the row associated with the address (Col. 2, lines 43-48), further comprising a stand-by mode comprising replacing step (c) with the steps of: (d) providing, by a dedicated circuit (500, Figure 15), a cyclic succession of offset values (Col. 11, lines 29-50; Col. 13, lines 52-67).

However, Richards does not teach that the cyclic succession of offset values is provided at a frequency proportional to the display frequency. However, Glennon describes that the cyclic succession of offset values is provided at a frequency proportional to the display frequency (Col. 3, lines 51-65; Col. 3, lines 30-33).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Richards so that the cyclic succession of offset values is provided at a frequency proportional to the display frequency as suggested by Glennon because

Glennon suggests that this is needed in order to achieve the appearance of smooth motion (Col. 3, line 66-Col. 4, line 3).

However, Richards and Glennon do not teach (e) for each row address of the frame memory, activating pixels of a screen line associated with the address offset by a same pixel position offset value, based on the read states of the row associated with the address. However, Wu discloses (e) for each row address of the frame memory, activating pixels of a screen line associated with the address offset by a same pixel position offset value, based on the read states of the row associated with the address (*Each scan line is a row of pixels wherein the data related to each pixel is stored in a location in frame buffer 202. The locations storing pixel data in frame buffer 202 are typically arranged such that their order corresponds to the sequential order of the pixels in the scan lines of a monitor screen. Such an order allows pixel data to be conveniently retrieved and sent to the display monitor. MIU 207 computes the next address by adding/subtracting an offset value of 128 data bits in the current mode to/from the present address*, Col. 9, lines 11-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Richards and Glennon so that (e) for each row address of the frame memory, activating pixels of a screen line associated with the address offset by a same pixel position offset value, based on the read states of the row associated with the address as suggested by Wu because Wu suggests that computing the address slows down the processing speed and increases the power consumption (Col. 2, lines 19-24), and therefore obtaining the address by address offsets (Col. 3, lines 1-9) increases the processing speed and decreases the power consumption (Col. 2, lines 32-36).

26. Claims 2, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Richards (US006756976B2) in view of Glennon (US006359654B1), further in view of Leung (US005900887A), further in view of Wu (US006414689B1).

27. With regard to Claim 2, Richards describes a device for displaying an image on an array screen comprising a frame memory (310, Figure 2a) comprising memory points arranged in rows and in columns (Col. 5, lines 61-65; Col. 13, lines 45-51; Col. 17, lines 47-49); a write means for storing in the frame memory an image in digital form (Col. 2, lines 43-48; Col. 3, lines 4-6); a read means for reading the states of the memory points of a row of the frame memory at a determined row address (Col. 3, lines 39-42); a row driver (402, Figure 3) for selecting a screen LINE based on the determined row address (Col. 3, lines 31-34); and a column driver for activating pixels of the selected line based on the states of memory points read by the read means, further comprising a dedicated control circuit (500, Figure 15) for providing a cyclic succession of offset values (Col. 11, lines 29-50; Col. 13, lines 52-67); and a dedicated address circuit (406, Figure 9) receiving the address of the row read by the read means (Col. 3, lines 39-42) and transmitting to the row driver a new address (Col. 3, lines 31-34).

However, Richards does not teach that the cyclic succession of offset values is provided at a frequency proportional to the display frequency. However, Glennon describes that the cyclic succession of offset values is provided at a frequency proportional to the display frequency (Col. 3, lines 51-65; Col. 3, lines 30-33), as discussed in the rejection for Claim 1.

However, Richards and Glennon do not teach a column driver for activating pixels of the selected line based on the states of memory points. However, Leung describes a column driver for activating pixels of the selected line based on the states of memory points (Col. 2, lines 2-9, 64-67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Richards and Glennon to include a column driver for activating pixels of the selected line based on the states of memory points as suggested by Leung because Leung suggests the advantage of not having to write each pixel location, but can write larger blocks of pixel at the same time (Col. 1, lines 35-42; Col. 2, lines 2-9, 64-67).

However, Richards and Glennon do not teach that the new address corresponds to the address of the read row offset by a same pixel position offset value. However, Wu discloses the new address corresponds to the address of the read row offset by a same pixel position offset value (*data related to each pixel is stored in a location in frame buffer 202, MIU 207 computes the next address by adding/subtracting an offset value of 128 data bits in the current mode to/from the present address,* Col. 9, lines 11-45). This would be obvious for the same reasons given in the rejection for Claim 1.

28. With regard to Claim 4, Richards does not teach that the dedicated address circuit is an adder adapted to adding the pixel position offset value to the address of the read row. However, Wu discloses that the dedicated address circuit is an adder adapted to adding the pixel position offset value to the address of the read row (*data related to each pixel is stored in a location in frame buffer 202, MIU 207 computes the next address by adding an offset value of 128 data bits*

in the current mode to/from the present address, Col. 9, lines 11-45). This would be obvious for the same reasons given in the rejection for Claim 1.

29. With regard to Claim 5, Richards describes that the screen is a screen with light-emitting diodes (Col. 2, lines 32-36).

30. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 20030076332A1) in view of Chen (US005613048A).

Choi is relied upon for the teachings as discussed above relative to Claim 11.

However, Choi does not teach that displaying the substantially similar or identical image at different pixel positions at different times is perceptible to a human as motion of the image. However, Chen discloses that displaying the substantially similar or identical image at different pixel positions at different times is perceptible to a human as motion of the image (*A pixel 20, or a group of pixels, is identified in one of the images, and the location of the same pixel or group of pixels is determined in the second image. The displacement of the pixel 20 in going from image A to image B is used to form an offset map*, Col. 4, lines 20-30; *generation of images representing different locations of a virtual camera, the camera might be movable in two-dimension or three-dimensional space*, Col. 3, lines 14-27).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi so that displaying the substantially similar or identical image at different pixel positions at different times is perceptible to a human as motion of the image as suggested by Chen because Chen suggests the advantage of enabling a continuous

sequence of new images that independent of scene complexity and which do not require specialized hardware to implement to be generated rapidly on a real-time basis (Col. 1, lines 64-Col. 2, line 2).

31. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 20030076332A1) in view of Werner (US006545740B2).

Choi is relied upon for the teachings as discussed above relative to Claim 13.

However, Choi does not teach that the position of the substantially similar or identical image is changed at a frequency that is approximately a multiple of a frame rate at which the image is displayed. According to the disclosure of this application, this occurs during a faster general motion (page 6, lines 1-10). Werner discloses inserting more image frames into the series in order to double the frame rate (Col. 8, lines 11-14). These image frames show the same object that is moved from frame to frame (Col. 6, lines 39-41). This avoids a slow motion effect that otherwise would occur if the same frame rate is to be used (Col. 8, lines 8-14). Therefore, Werner discloses that the position of the substantially similar or identical image is changed at a frequency that is approximately a multiple of a frame rate at which the image is displayed (Col. 8, lines 5-29).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi so that the position of the substantially similar or identical image is changed at a frequency that is approximately a multiple of a frame rate at which the image is displayed as suggested by Werner because Werner suggests that this is advantageous

when an object is moving rapidly because it diminishes the flicker effects of frame objects (Col. 1, lines 47-48; Col. 8, lines 5-29).

32. Claims 15, 16, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 20030076332A1) in view of Tsuda (US 20020180673A1).

33. With regard to Claim 15, Choi is relied upon for the teachings as discussed above relative to Claim 6.

However, Choi does not teach entering a stand-by mode in response to determining that the second image is substantially similar or identical to the first image. However, Tsuda discloses entering a stand-by mode in response to determining that the second image is substantially similar or identical to the first image (*when displaying a static image, or a moving picture which is not being moved fast, a long quiescent period T2 is set for the non-scanning period, so that power consumption for rewriting the screen can be reduced,* [0260]).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi to include entering a stand-by mode in response to determining that the second image is substantially similar or identical to the first image as suggested by Tsuda because Tsuda suggests the advantage of obtaining an optimal low power consumption for each type of display image [0260].

34. With regard to Claim 16, Choi does not teach that the stand-by mode comprises displaying a substantially similar or identical image at different pixel positions on the display at

different times. However, Tsuda discloses that the stand-by mode comprises displaying a substantially similar or identical image at different pixel positions on the display at different times (*when displaying a moving picture which is not being moved fast, power consumption is reduced*, [0260]). This would be obvious for the same reasons given in the rejection for Claim 15.

35. With regard to Claim 23, Claim 23 is similar in scope to Claim 16, and therefore is rejected under the same rationale.

36. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 20030076332A1) in view of Cupps (US006976180B2).

Choi is relied upon for the teachings as discussed above relative to Claim 6.

However, Choi does not teach entering a stand-by mode in response to determining that no user input has been received for a determined period of time. However, Cupps discloses entering a stand-by mode in response to determining that no user input has been received for a determined period of time (*System processor 302 waits for a period of time, then powers down display 307 to conserve power. System processor 302 is then in its "standby" mode, idling and waiting for user input*, Col. 10, lines 52-56).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi to include entering a stand-by mode in response to determining that no user input has been received for a determined period of time as suggested by Cupps because Cupps suggests the advantage of conserving power (Col. 10, lines 42-56) in

mobile devices so that the mobile device can have a small size while having enough power to operate (Col. 1, lines 34-47).

37. Claims 21 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 20030076332A1) in view of Wu (US006414689B1).

38. With regard to Claim 21, Choi is relied upon for the teachings as discussed above relative to Claim 20. Choi discloses that direction information that indicates at least one direction in which a display position of the image is to be offset (*sends the control signal, which causes the displayed image to move by one pixel in the left direction*, [0036]).

However, Choi does not teach that the position offset information comprises row and/or column offset information. However, Wu discloses that the position offset information comprises row and/or column offset information (*data related to each pixel is stored in a location in frame buffer 202, the address is determined by adding one 128-bits boundary to the present address which is represented by the packet in the first row*, Col. 9, lines 11-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi so that the position offset information comprises row and/or column offset information as suggested by Wu because Wu suggests that displays are activated by rows, and therefore the position offset information must include row offset information in order to activate the correct row (Col. 9, lines 11-45).

39. With regard to Claim 25, Choi does not teach at least one third circuit that receives address information about the location within the memory at which information about the image is stored and also receives the position offset information, wherein the third circuit determines offset address information based on the address information and the offset information, and provides the offset address information to the at least one first circuit. However, Wu discloses at least one third circuit (207, Figure 2) that receives address information about the location within the memory at which information about the image is stored (*provide destination pixel address information to MIU 207 to retrieve data from frame buffer 202*, Col. 6, lines 19-22) and also receives the position offset information, wherein the third circuit determines offset address information based on the address information and the offset information, and provides the offset address information to the at least one first circuit (208) (*because 128 data bits are to be rendered by GE 301 as indicated by bit AO being HIGH, MIU 207 computes the next address by adding/subtracting an offset value of 128 data bits to/from the present address*, Col. 9, lines 11-45; *display controller 208 retrieves image data from frame buffer 202 via MIU 207*, Col. 5, lines 48-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi to include at least one third circuit that receives address information about the location within the memory at which information about the image is stored and also receives the position offset information, wherein the third circuit determines offset address information based on the address information and the offset information, and provides the offset address information to the at least one first circuit as suggested by Wu because Wu

suggests that this is needed in order to retrieve the correct data from the correct location in memory (Col. 9, lines 11-45).

40. With regard to Claim 26, Choi does not teach that the at least one third circuit comprises an arithmetic logic unit. However, Wu discloses that the at least one third circuit (207, Figure 2) comprises an arithmetic logic unit (*MIU 207 computes the next address by adding/subtracting*, Col. 9, lines 11-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi so that the at least one third circuit comprises an arithmetic logic unit as suggested by Wu because Wu suggests that arithmetic logic unit is needed in order to select rows (Col. 9, lines 11-45).

41. With regard to Claim 27, Choi does not teach at least one fourth circuit that receives image information and the offset information and determines offset image information based on the image information and the offset information, and provides the offset image information to the at least one first circuit. However, Wu discloses at least one fourth circuit (301, Figure 3) that receives image information and the offset information and determines offset image information based on the image information and the offset information, and provides the offset image information to the at least one first circuit (208, Figure 2) (*the starting address and other information related to this data such as the number of data bits per pixel is communicated to GE 301*, Col. 6, line 62-Col. 7, line 12, *GE 301 is not yet at EOL, as indicated by bit EOL being LOW. Because 128 data bits are to be rendered by GE 301 as indicated by bit AO being HIGH,*

MIU 207 computes the next address by adding/subtracting an offset value, Col. 9, lines 11-45; *display controller 208 retrieves image data from frame buffer 202 via MIU 207*, Col. 5, lines 48-51).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi to include at least one fourth circuit that receives image information and the offset information and determines offset image information based on the image information and the offset information, and provides the offset image information to the at least one first circuit as suggested by Wu because Wu suggests that this is needed in order to make sure that the image data that is accessed is ready to be displayed (Col. 9, lines 11-45).

42. With regard to Claim 28, Choi does not teach that the at least one fourth circuit comprises a register. However, Wu discloses that the at least one fourth circuit (301, Figure 3) comprises a register (*registers inside GE 301*, Col. 6, line 63-Col. 7, line 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi so that the at least one fourth circuit comprises a register as suggested by Wu because Wu suggests that the registers are needed in order to the data in advance to increase the processing speed (Col. 6, line 63-Col. 7, line 2).

43. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 20030076332A1) and Tsuda (US 20020180673A1) in view of Cupps (US006976180B2).

Claim 24 is similar in scope to Claim 17, and therefore is rejected under the same rationale.

44. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Choi (US 20030076332A1) in view of Richards (US006756976B2).

Choi is relied upon for the teachings as discussed above relative to Claim 29.

However, Choi does not teach that activating the pixels comprises activating light-emitting diodes to display the image. However, Richards discloses that activating the pixels comprises activating light-emitting diodes to display the image (Col. 2, lines 32-36).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Choi so that activating the pixels comprises activating light-emitting diodes to display the image as suggested by Richards because Richards suggests that LEDs are advantageous for field-sequential color displays because LEDs may simply be switched on and off as desired (Col. 2, lines 32-36).

Allowable Subject Matter

45. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

46. The prior art taken singly or in combination do not teach or suggest the device of Claim 2 wherein the dedicated state circuit is a shift register, in which are written the states of memory

points provided by the read means, adapted to performing an offset by a determined number of bits on the states, as recited in Claim 3.

47. The closest prior art (Cairns US006806854B2) teaches a shift register (25, Figure 8), in which are written the states of memory points (Col. 8, lines 10-32). However, Cairns does not teach that the shift register is adapted to performing an offset by a determined number of bits on the states.

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cairns (US006806854B2) teaches an active matrix display comprising an active matrix of N rows and M columns of pixels and a driver for driving the pixels (Col. 1, lines 14-27).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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